IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

receiving power control instructions via a first link in a first plurality of frames;

keeping a running history, up to a predetermined length, of the received power control instructions ~~included in a first plurality frames received in one direction on a link of a channel, the first frames being queued before processing~~; and

generating power control ~~commands~~ bits for transmission via a second link in a second plurality of frames ~~to be transmitted on a return direction of the channel~~, the power control bits being generated based at least in part on the running history being kept for the power control instructions received via the first link, ~~in a manner that effectuates a slowing of response to the incoming power control instructions, the second frames also being batched for subsequent processing in batch form for transmission, wherein the power control instructions and commands are in a form of power control bits, and the predetermined length equals two bits and wherein the generating comprises generating~~ wherein m "zero" value power control bits and n "one" value power control bits are generated for each batch formed with a subset of the second plurality of frames, with ~~m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10",~~ m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history~~, such that if each batch of the subset of the second frames contains an even number of frames, m and n are equal~~.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Currently Amended) The method of claim 1, wherein m and n differ by 1 if each batch of the subset of the second plurality of frames contains an odd number of frames and if

the number of power control instructions with "0" value is equal to the number of power control instructions with "1" value in the running history~~, m and n differ by 1~~.

6. (Original) The method of claim 5, wherein m is greater than n by 1 for batches of odd ordinal positions in their order of formation, and n is greater than m by 1 for batches of even ordinal positions in their order of formation.

7. (Previously presented) The method of claim 5, wherein m is greater than n by 1 for batches of even ordinal positions in their order of formation, and n is greater than m by 1 for batches of odd ordinal positions in their order of formation.

8. (Currently Amended) The method of claim 1, wherein said generating comprises alternating between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second plurality of frames~~, with a selected one of the last frame and the last two frames receiving a "one" value power control bit, if the two bits running history equal "11"~~.

9. (Currently Amended) The method of claim 1~~-8~~, wherein if the running history includes two power control instructions of "11" for two frames received via the first link, ~~the last frame receives a~~ each batch includes one extra "one" value power control bit~~,~~ if there are odd number of frames in each batch, and ~~the last two frames receive a~~ each batch includes two extra "one" value power control bits ~~bit,~~ if there are even number of frames in each batch.

10. (Currently Amended) The method of claim 1, wherein each batch includes equal number of "zero" value power control bits and "one" value power control bits if the running history includes two power control instructions of "01" or "10" for two frames received via the first link and if there are even number of frames in each batch ~~said generating comprises alternating between generating "zero" value power control bit and "one" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "zero" value power control bit, if the two bits running history equal "00"~~.

11. (Currently Amended) The method of claim 1 ~~10~~, wherein if the running history includes two power control instructions of "00" for two frames received via the first link, ~~the last frame receives a~~ each batch includes one extra "zero" value power control bit~~,~~ if there are odd number of frames in each batch, and ~~the last two frames receive a~~ each batch includes two extra "zero" value power control bits ~~bit,~~ if there are even number of frames in each batch.

12. (Original) The method of claim 1, wherein said keeping and generating operations are being performed in a gateway of a wireless communication system.

13. (Original) The method of claim 1, wherein said keeping and generating operations are being performed in an emulated gateway and a gateway simulator of a wireless communication test system.

14. (Currently Amended) A gateway of a wireless communication system, comprising:

a transceiver to receive power control instructions in a first plurality of frames on a first link ~~of a channel, and batch said first frames for processing in batch, each of said first frames include a power control instruction, and the transceiver outputting the power control instruction included in each of said first frames~~; and

a processing subsystem coupled to the transceiver subsystem ~~to process the batched first frames in batch and~~ to receive the power control instructions ~~of the first frames~~ outputted by the transceiver ~~subsystem~~, ~~and to generate a second plurality of frames for a second link of the channel, the second plurality of frames also being batched before being handled by the transceiver subsystem in batch, wherein the processing subsystem is adapted to:~~

to keep a running history, up to a predetermined length, of the received power control instructions ~~included in the first frames~~, ~~and~~

to generate power control bits ~~commands~~ for transmission via a second link in a ~~the~~ second plurality of frames, to generate the power control bits based at least in part on the running history being kept for the received power control instructions, ~~in a manner that effectuates slowing of responding to the incoming power control instructions;~~

~~wherein the processing subsystem is further adapted~~ and to generate m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second plurality of frames, with ~~m and n differ by at most 1, if the two bits running history equals a selected one of "01" and "10",~~ m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history ~~and wherein the processing subsystem is further adapted to generate equal number of "zero" value and "one" value power control bits, if each batch of the subset of the second frames contains an even number of frames,~~

~~wherein the power control instructions are in a form of power control bits, and the predetermined length equals two bits~~.

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Currently Amended) The gateway of claim 14, wherein the processing subsystem ~~is designed to generate a selected one of~~ generates either one more "zero" value power control bit ~~and~~ or one more "one" value power control bit~~,~~ ~~if~~ for each batch of the subset of the second plurality of frames if each batch contains an odd number of frames and if the number of power control instructions with "0" value is equal to the number of power control instructions with "1" value in the running history.

19. (Original) The gateway of claim 18, wherein the processing subsystem is designed to generate one more "zero" value power control bit for batches of odd ordinal positions in their order of formation, and one more "one" value power control bit for batches of even ordinal positions in their order of formation.

20. (Previously presented) The gateway of claim 18, wherein the processing subsystem is designed to generate one more "zero" value power control bit for batches of

even ordinal positions in their order of formation, and one more "one" value power control bit for batches of odd ordinal positions in their order of formation.

21. (Currently Amended) The gateway of claim 14, wherein the processing subsystem ~~is designed to alternate~~ alternates between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second plurality of frames~~, with a selected one of the last frame and the last two frames receiving a "one" value power control bit, if the two bits running history equal "11"~~.

22. (Currently Amended) The gateway of claim 14~~ 21~~, wherein if the running history includes two power control instructions of "11" for two frames received via the first link, the processing subsystem ~~is designed to generate the last frame with a~~ generates one extra "one" value power control bit in each batch~~,~~ if there are odd number of frames in each batch~~,~~ and ~~the last two frames with a~~ generates two extra "one" value power control bits in each batch ~~bit,~~ if there are even number of frames in each batch.

23. (Currently Amended) The gateway of claim 14, wherein the processing subsystem generates equal number of "zero" value power control bits and "one" value power control bits for each batch if the running history includes two power control instructions of "01" or "10" for two frames received via the first link and if there are even number of frames in each batch ~~is designed to alternate between generating "zero" value power control bit and "one" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "zero" value power control bit, if the two bits running history equal "00"~~.

24. (Currently Amended) The gateway of claim 14~~ 23~~, wherein if the running history includes two power control instructions of "00" for two frames received via the first link, the processing subsystem ~~is designed to generate the last frame with a~~ generates one extra "zero" value power control bit in each batch~~,~~ if there are odd number of frames in each batch~~,~~ and ~~the last two frames with a~~ generates two extra "zero" value power control bits in each batch ~~bit,~~ if there are even number of frames in each batch.

25. (Currently Amended) A wireless communication testing system, comprising:

a gateway emulator to emulate a gateway including receipt of power control instructions in a first plurality frames ~~in one direction~~ on a first link ~~of a channel, and queuing said first frames for processing in batch, each of said first frames including a power control instruction, and the gateway emulator outputting the power control instruction included in each of said first frames~~; and

a gateway simulator coupled to the gateway emulator ~~to process the grouped first frames in batch and~~ to receive the power control instructions ~~of the first frames output by~~ from the gateway emulator, ~~and to generate a second plurality of frames for transfer in an opposite direction on a link of the channel, the second plurality of frames also being batched before being handled by the gateway emulator in batch, wherein the gateway simulator is designed to:~~

to maintain a running history, over a predetermined length, of the received power control instructions ~~included with the first frames, and~~

to generate power control bits ~~commands~~ for transmission via a second link in a ~~the~~ second plurality of frames, to generate the power control bits based at least in part on the running history being kept for the received power control instructions, ~~in a manner that effectuates a slowing of response to the incoming power control instructions;~~

~~wherein the power control instructions and commands are in a form of power control bits of a predetermined length equal to two bits, and wherein the gateway simulator is further designed to:~~

and to generate m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second plurality of frames, with ~~m and n differing by at most 1, if the two bits running history equals a selected one of "01" and "10",~~ m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history; ~~and~~

~~generate an equal number of "zero" value and "one" value power control bits, if each batch of the subset of the second frames contains an even number of frames~~.

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Currently Amended) The wireless communication testing system of claim 25, wherein the gateway simulator ~~is designed to generate a selected one of~~ generates either one more "zero" value power control bit ~~and~~ or one more "one" value power control bit~~,~~ ~~if~~ for each batch of the subset of the second plurality of frames if each batch contains an odd number of frames and if the number of power control instructions with "0" value is equal to the number of power control instructions with "1" value in the running history.

30. (Original) The wireless communication testing system of claim 29, wherein the gateway simulator is designed to generate one more "zero" value power control bit for batches of odd ordinal positions in their order of formation, and one more "one" value power control bit for batches of even ordinal positions in their order of formation.

31. (Previously presented) The wireless communication testing system of claim 29, wherein the gateway simulator is designed to generate one more "zero" value power control bit for batches of even ordinal positions in their order of formation, and one more "one" value power control bit for batches of odd ordinal positions in their order of formation.

32. (Currently Amended) The wireless communication testing system of claim 25 ~~26~~, wherein the gateway simulator ~~is designed to alternate~~ alternates between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second plurality of frames~~, with a selected one of the last frame and the last two frames receiving a "one" value power control bit, if the two bits running history equal "11"~~.

33. (Currently Amended) The wireless communication testing system of claim 25 ~~32~~, wherein if the running history includes two power control instructions of "11" for two frames received via the first link, the gateway simulator ~~is designed to generate the last frame with a~~ generates one extra "one" value power control bit in each batch~~,~~ if there are odd

number of frames in each batch~~,~~ and ~~the last two frames with a~~ generates two extra "one" value power control bits in each batch ~~bit,~~ if there are even number of frames in each batch.

34. (Currently Amended) The wireless communication testing system of claim 25 ~~26~~, wherein the gateway simulator generates equal number of "zero" value power control bits and "one" value power control bits for each batch if the running history includes two power control instructions of "01" or "10" for two frames received via the first link and if there are even number of frames in each batch ~~is designed to alternate between generating "zero" value power control bit and "one" value power control bit for each batch formed with a subset of the second frames, with a selected one of the last frame and the last two frames receiving a "zero" value power control bit, if the two bits running history equal "00"~~.

35. (Currently Amended) The wireless communication testing system of claim 25 ~~34~~, wherein if the running history includes two power control instructions of "00" for two frames received via the first link, the gateway simulator ~~is designed to generate the last frame with a~~ generates one extra "zero" value power control bit in each batch~~,~~ if there are odd number of frames in each batch~~,~~ and ~~the last two frames with a~~ generates two extra "zero" value power control bits in each batch ~~bit,~~ if there are even number of frames in each batch.

36. (Currently Amended) Apparatus comprising:

means for receiving power control instructions via a first link in a first plurality of frames;

means for keeping a running history, up to a predetermined length, of the received power control instructions ~~included in a first plurality frames received on a first link of a channel, the first frames being grouped before their processing~~; and

means for generating power control bits ~~commands~~ for transmission via a second link in a second plurality of frames ~~to be transmitted on a second link of the channel~~, the power control bits being generated based at least in part on the running history being kept for the power control instructions received via the first link, ~~in a manner that effectuates a slowing response to the incoming power control instructions, the second frames also being grouped for subsequent processing in batch for transmission, wherein the power control instructions and commands are in a form of power control bits, and the predetermined length equals two~~

~~bits and wherein the means for generating power control commands comprises generating~~ wherein m "zero" value power control bits and n "one" value power control bits are generated for each batch formed with a subset of the second plurality of frames, with ~~m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10",~~ m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history ~~and wherein the means for generating power control commands comprises generating equal number of "zero" value and "one" value power control bits, if each batch of the subset of the second frames contains an even number of frames~~.

37. (Currently Amended) A machine readable medium having stored thereon machine executable instructions that when executed implement a method comprising:

receiving power control instructions via a first link in a first plurality of frames;

keeping a running history, up to a predetermined length, of the received power control instructions ~~included in a first plurality frames received on a first link of a channel, the first frames being grouped before their processing~~; and

generating power control bits ~~commands~~ for transmission via a second link in a second plurality of frames ~~to be transmitted on a second link of the channel~~, the power control bits being generated based at least in part on the running history being kept for the power control instructions received via the first link, ~~in a manner that effectuate slowing response to the incoming power control instructions, the second frames also being grouped for subsequent processing in batch for transmission, wherein the power control instructions and commands are in a form of power control bits, and the predetermined length equals two bits and wherein the generating step comprises generating~~ wherein m "zero" value power control bits and n "one" value power control bits are generated for each batch formed with a subset of the second plurality of frames, with ~~m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10",~~ m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history ~~and wherein the power control commands for the second plurality of frames comprises an equal number of "zero" value and "one" value power control bits, if each batch of the subset of the second frames contains an even number of frames~~.

38. (Currently Amended) A machine readable medium having stored thereon machine executable instructions that when executed implement a method comprising:

emulating a gateway including receipt of power control instructions in a first plurality frames on a first link ~~of a channel, and grouping said first frames for processing in batch form, each of said first frames including a power control instruction, and outputting the power control instruction includes in each of said first frames~~;

emulating a gateway simulator ~~coupled to the gateway emulator to process the batched first frames in batch and~~ to receive the power control instructions ~~of the first frames outputted by the gateway emulator, and to generate a second plurality of frames for a second link of the channel, the second plurality of frames also being batched before being handled by the gateway emulator in batch, wherein the gateway simulator is adapted to:~~

to keep a running history, up to a predetermined length, of the received power control instructions ~~included in the first frames~~, ~~and~~

to generate power control bits ~~commands~~ for transmission via a second link in a ~~the~~ second plurality of frames, to generate the power control bits based at least in part on the running history being kept for the power control instructions received via the first link, ~~in a manner that effectuates slowing of responding to the incoming power control instructions, wherein the power control instructions and power control commands are in a form of power control bits, and the predetermined length equals two bits and wherein the generating step comprises generating~~ and to generate m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second plurality of frames, with ~~m and n differing by at most 1, if the two-bit running history equals a selected one of "01" and "10",~~ m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history, ~~and wherein the power control commands for the second frames comprise equal number of "zero" value and "one" value power control bits, if each batch of the subset of the second frames contains an even number of frames~~.